Configuring Frequency Synchronization

Table 1: Feature History Table

Feature name	Release Information	Feature Description
Synchronous Ethernet (SyncE) Support on 88-LC0-36FH-M Line card and 8202-32FH-M Router	Release 7.5.2	With this release, support for Synchronous Ethernet (SyncE) ITU-T profiles G.8262 and G.8264 is extended to the following: • 88-LC0-36FH-M line card • 8202-32FH-M router The SyncE profile G.8262 enables synchronous ethernet clock support and the SyncE profile G.8264 enables ethernet synchronization messaging channel (ESMC).
Support for Frequency Synchronization	Release 7.3.1	Based on the ITU-T G.8262 recommendations, precision frequency is enabled on timing devices to deliver frequency synchronization for bandwidth, frequency accuracy, holdover, and measure noise generation. This support allows for correct network operations when synchronous equipment is timed from either another synchronous equipment clock or a higher-quality clock.

Overview

Frequency synchronization is the ability to distribute precision frequency around a network. In this context, timing refers to precision frequency, not an accurate time of day. Precision frequency is required in next generation networks for applications such as circuit emulation.

To achieve compliance to ITU specifications for TDM, differential method circuit emulation must be used, which requires a known, common precision frequency reference at each end of the emulated circuit. This is used in conjunction with an external timing technology to provide synchronization of precision timing across the network.

SDH equipments are widely replaced by Ethernet equipments and synchronized frequency is required over such Ethernet ports. Synchronous Ethernet (SyncE) is used to accurately synchronize frequency in devices connected by Ethernet in a network. SyncE provides level frequency distribution of known common precision frequency references to a physical layer Ethernet network.

To maintain SyncE links, a set of operational messages are required. These messages ensure that a node is always deriving timing information from the most reliable source and then transfers the timing source quality information to clock the SyncE link.

Source and Selection Points

Frequency Synchronization implementation involves Sources and Selection Points.

A Source inputs frequency signals into a system or transmits them out of a system. There are four types of sources:

- Line interfaces. This includes SyncE interfaces.
- Clock interfaces. These are external connectors for connecting other timing signals, such as BITS and GPS.
- PTP clock. If IEEE 1588 version 2 is configured on the router, a PTP clock may be available to frequency synchronization as a source of the time-of-day and frequency.
- Internal oscillator. This is a free-running internal oscillator chip.

Each source has a Quality Level (QL) associated with it which gives the accuracy of the clock. This provides information about the best available source the devices in the system can synchronize to. To define a predefined network synchronization flow and prevent timing loops, you can assign priority values to the sources on each router. The combination of QL information and user-assigned priority levels allow each router to choose a source to synchronize its SyncE interfaces, as described in the ITU standard G.781.

A Selection Point is any point where a choice is made between several frequency signals and possibly one or many of them are selected. Selection points form a graph representing the flow of timing signals between different cards in a router running Cisco IOS XR software. For example, there can be one or many selection points between different Synchronous Ethernet inputs available on a single line card. This information is forwarded to a selection point on the router, to choose between the selected source from each card.

The input signals to the selection points can be:

- Received directly from a source.
- Received as the output from another selection point on the same card.
- Received as the output from a selection point on a different card.

The output of a selection point can be used in a number of ways, like:

- To drive the signals sent out of a set of interfaces.
- As input into another selection point on a card.
- As input into a selection point on an another card.

Use **show frequency synchronization selection** command to see a detailed view of the different selection points within the system.

Note

- We recommend you to configure, and enable Frequency Synchronization selection input on two interfaces per line card.
- For link aggregation, you must configure and enable Frequency Synchronization selection input on a single bundle member.

SyncE Profiles Support Matrix

This table provides information on the SyncE profiles that are supported on the Cisco 8000 series routers and line cards.

Table 2: SyncE Profiles Support Matrix

SyncE Restrictions

This section lists a restriction in configuring frequency synchronization.

- SyncE is not supported on 8800-RP 1588 ports.

Enabling Frequency Synchronization on the Router

This task describes the router-level configuration required to enable frequency synchronization.

Note If timing mode system is not configured, the major alarm `T4 PLL is in FREERUN mode` is raised. This alarm has no functional impact to the system behavior.

SUMMARY STEPS

1. **configure**
2. **frequency synchronization**
3. **clock-interface timing-mode** {**independent** | **system**
4. **quality itu-t option** {**1** | **2 generation** {**1** | **2**}}
5. **log selection** {**changes** | **errors**}
6. Use one of these commands:

- **end**
- **commit**

DETAILED STEPS

	Command or Action	Purpose
Step 1	**configure** **Example:** `RP/0/RP0/CPU0:router# configure`	Enters mode.
Step 2	**frequency synchronization** **Example:** `Router(config)# frequency synchronization`	Enables frequency synchronization on the router.
Step 3	**clock-interface timing-mode** {**independent** | **system** **Example:** `Router(config-freqsync)# clock-interface timing-mode system`	Configures the type of timing sources that can be used to drive the output from a clock interface. If this command is not used, the default quality mode is used. In the default mode, the clock interface output is driven only by input from line interfaces and the internal oscillator; it is never driven by input from another clock interface. In addition, some heuristic tests are run to detect if the signal being sent out of one clock interface can be looped back by some external box and sent back in via the same, or another clock interface. • **independent**—Specifies that the output of clock interfaces is driven only by the line interfaces (SyncE), as in the default mode. Loopback detection is disabled. • **system**—Specifies that the output of a clock interface is driven by the system-selected timing source (the source used to drive all SyncE interfaces), including clock interfaces. Loopback detection is disabled.
Step 4	**quality itu-t option** {**1** | **2 generation** {**1** | **2**}} **Example:** `Router(config-freqsync)# quality itu-t option 2 generation 1`	(Optional) Specifies the quality level for the router. The default is **option 1**. • **option 1**—Includes PRC, ePRTC, PRTC, SSU-A, SSU-B, SEC, eEEC, and DNU. • **option 2 generation 1**—Includes PRS, ePRTC, PRTC, STU, ST2, ST3, SMC, ST4, eEEC, and DUS. • **option 2 generation 2**—Includes PRS, ePRTC, PRTC, STU, ST2, ST3, ST3E, SMC, ST4,XeEEC, and DUS. **Note** `The quality option configured here must match the quality option specified in the **quality receive** and **quality transmit** commands in interface frequency synchronization configuration mode.

	Command or Action	Purpose
Step 5	**log selection** {**changes** | **errors**} **Example:** `Router(config-freqsync)# log selection changes`	Enables logging to frequency synchronization. • **changes**—Logs every time there is a change to the selected source, in addition to errors. • **errors**—Logs only when there are no available frequency sources, or when the only available frequency source is the internal oscillator.

Step 6	Use one of these commands:
	• **end**
	• **commit**
	Example:
	`Router(config-freqsync)# end`
	or
	`Router(config-freqsync)# commit`
		Saves configuration changes.
		• When you issue the **end** command, the system prompts you to commit changes:
		`Uncommitted changes found, commit them before exiting(yes/no/cancel)? [cancel]:`
		• Entering **yes** saves configuration changes to the running configuration file, exits the configuration session, and returns the router to EXEC mode.
		• Entering **no** exits the configuration session and returns the router to EXEC mode without committing the configuration changes.
		• Entering **cancel** leaves the router in the current configuration session without exiting or committing the configuration changes.
		• Use the **commit** command to save the configuration changes to the running configuration file, and remain within the configuration session.

What to do next

Configure frequency synchronization on any interfaces that should participate in frequency synchronization.

Configuring Frequency Synchronization on an Interface

By default, there is no frequency synchronization on line interfaces. Use this task to configure an interface to participate in frequency synchronization.

Before you begin

You must enable frequency synchronization globally on the router.

SUMMARY STEPS

1. **configure**
2. **interface** *type interface-path-id*

3. **frequency synchronization**
4. **selection input**
5. **priority** *priority-value*
6. **wait-to-restore** *minutes*
7. **ssm disable**
8. **time-of-day-priority** *priority*
9. **quality transmit** {**exact** | **highest** | **lowest**} **itu-t option** *ql-option*
10. **quality receive** {**exact** | **highest** | **lowest**} **itu-t option** *ql-option*
11. Use one of these commands:
    - **end**
    - **commit**

DETAILED STEPS

	Command or Action	Purpose
Step 1	**configure** **Example:** `RP/0/RP0/CPU0:router# configure`	Enters mode.
Step 2	**interface** *type interface-path-id* **Example:** `Router(config)# interface HundredGigE 0/1/1/0`	Enters interface configuration mode.
Step 3	**frequency synchronization** **Example:** `Router(config-if)# frequency synchronization`	Enables frequency synchronization on the interface and enters interface frequency synchronization mode to configure the various options. By default, this causes the system selected frequency signal to be used for clocking transmission, but does not enable the use of the interface as an input.
Step 4	**selection input** **Example:** `Router(config-if-freqsync)# selection input`	(Optional) Specifies the interface as a timing source to be passed to the selection algorithm.
Step 5	**priority** *priority-value* **Example:** `Router(config-if-freqsync)# priority 100`	(Optional) Configures the priority of the frequency source on a controller or an interface. Values can range from 1 (highest priority) to 254 (lowest priority). The default value is 100. This command is used to set the priority for an interface or clock interface. The priority is used in the clock-selection algorithm to choose between two sources that have the same quality level (QL). Lower priority values are preferred.
Step 6	**wait-to-restore** *minutes* **Example:**	(Optional) Configures the wait-to-restore time, in minutes, for frequency synchronization on an interface. This is the

	Command or Action	Purpose
	`Router(config-if-freqsync)# wait-to-restore 300`	amount of time after the interface comes up before it is used for synchronization. Values can range from 0 to 12. The default value is 5.
Step 7	**ssm disable** **Example:** `Router(config-if-freqsync)# ssm disable`	(Optional) Disables Synchronization Status Messages (SSMs) on the interface. • For SyncE interfaces, this disables sending ESMC packets, and ignores any received ESMC packets. • For clock interfaces, this causes DNUs to be sent, and ignores any received QL value.
Step 8	**time-of-day-priority** *priority* **Example:** `RP/0/RP0/CPU0:router(config-if-freqsync)# time-of-day-priority 50`	(Optional) Specifies the priority of this time source as the time-of-day (ToD) source. The priority is used as the first criterion when selecting between sources for a time-of-day selection point. Values can range from 1 (highest priority) to 254 (lowest priority); the default value is 100.
Step 9	**quality transmit** {**exact** | **highest** | **lowest**} **itu-t option** *ql-option* **Example:** `Router(config-clk-freqsync)# quality transmit highest itu-t option 1 prc`	(Optional) Adjusts the QL that is transmitted in SSMs. • **exact** *ql*—Specifies the exact QL to send, unless DNU would otherwise be sent. • **highest** *ql*—Specifies an upper limit on the QL to be sent. If the selected source has a higher QL than the QL specified here, this QL is sent instead. • **lowest** *ql*—Specifies a lower limit on the QL to be sent. If the selected source has a lower QL than the QL specified here, DNU is sent instead. The quality option specified in this command must match the globally-configured quality option in the **quality itu-t option** command. **Note** For clock interfaces that do not support SSM, only the lowest QL can be specified. In this case, rather than sending DNU, the output is squelched, and no signal is sent.
Step 10	**quality receive** {**exact** | **highest** | **lowest**} **itu-t option** *ql-option* **Example:** `Router(config-clk-freqsync)# quality receive highest itu-t option 1 prc`	(Optional) Adjusts the QL value that is received in SSMs, before it is used in the selection algorithm. • **exact** *ql*—Specifies the exact QL regardless of the value received, unless the received value is DNU. • **highest** *ql*—Specifies an upper limit on the received QL. If the received value is higher than this specified QL, this QL is used instead. • **lowest** *ql*—Specifies a lower limit on the received QL. If the received value is lower than this specified QL, DNU is used instead.

	Command or Action	Purpose
		The quality option specified in this command must match the globally-configured quality option in the **quality itu-t option** command. **Note** For clock interfaces that do not support SSM, only the exact QL can be specified.

Step 11	Use one of these commands:
	• **end**
	• **commit**
	Example:
	`Router(config-if-freqsync)# end`
	or
	`Router(config-if-freqsync)# commit`
		Saves configuration changes.
		• When you issue the **end** command, the system prompts you to commit changes:
		`Uncommitted changes found, commit them before exiting(yes/no/cancel)? [cancel]:`
		• Entering **yes** saves configuration changes to the running configuration file, exits the configuration session, and returns the router to EXEC mode.
		• Entering **no** exits the configuration session and returns the router to EXEC mode without committing the configuration changes.
		• Entering **cancel** leaves the router in the current configuration session without exiting or committing the configuration changes.
		• Use the **commit** command to save the configuration changes to the running configuration file, and remain within the configuration session.

Configuring Frequency Synchronization on a Clock Interface

External Timing Source

Clock interfaces are external connectors for connecting other timing signals, such as, GPS, BITS.

GPS

The router can receive 1PPS, 10 MHz, and ToD signals from an external clocking and timing source. The three inputs are combined as a Sync-2 interface to form the external timing source or the GPS input.

The GPS front panel connector details are:

- ToD—RS422 format as input
- 1PPS—RS422 or DIN connector as input
- 10MHz—DIN connector as input

GPS input starts only when all the three signals – 1PPS, 10MHz, and ToD are UP.

Note Unlike the Ethernet interface, the Sync-2 interface cannot receive or transmit QL. Ensure that you assign a QL value to the Sync-2 interface.

By default, 1PPS and 10MHz are in output mode. ToD output mode is not configurable.

For the variant, 8800-RP, 10MHZ and 1PPS can operate in output mode only when PTP Slave or BC mode are configured.

Note Both RP0 and RP1 should have identical configurations and should be connected to same external reference for sync 0 and sync 2 to meet phase transient response compliance standards during RP failover.

Configuring GPS Settings for the Grandmaster Clock

```
Router# configure
Router(config)# clock-interface sync 2 location 0/RP0/CPU0
Router(config-clock-if)# port-parameters
Router(config-clk-parms)# gps-input tod-format cisco pps-input ttl
Router(config-clk-parms)# exit
Router(config-clock-if)# frequency synchronization
Router(config-clk-freqsync)# selection input
Router(config-clk-freqsync)# wait-to-restore 0
Router(config-clk-freqsync)# quality receive exact itu-t option 1 PRC
Router(config-clk-freqsync)# exit
Router(config-clock-if)# frequency synchronization
Router(config-clk-freqsync)# quality itu-t option 1
Router(config-clk-freqsync)# clock-interface timing-mode system
Router(config-clk-freqsync)# end
```

Verifying the GPS Input

```
Router# show controllers timing controller clock

SYNCC Clock-Setting: -1 -1 6 -1
             Port 0    Port 1    Port 2    Port 3
Config :     No        No        Yes       No
Mode :       -         -         GPS       -
Submode1 :   -         -         CISCO     -
Submode2 :   -         -         UTC       -
Submode3 :   0         0         0         0
Shutdown :   0         0         0         0
Direction :  RX/TX     RX/TX     RX        RX/TX
Baud-Rate :  -         -         9600      -
QL Option :  O1        O1        -         -
RX_ssm(raw): -         -         -         -
TX_ssm :     -         -         -         -
If_state :   DOWN      DOWN      UP        DOWN  << Port 2 is UP when GPS input is valid.
```

When the front panel timing LED is Green, it indicates that the GPS is configured and 1PPS, ToD, and 10M iputs are valid.

Timing GPS LED Behavior:

- Timing GPS LED is off: Indicates no GPS is configured or the GPS port is down.

- Timing GPS LED is green: Indicates the GPS port is up.

SYNC LED Behavior:

- SYNC LED is green: Indicates that time core is synchronized to either external source, or SyncE or 1588.
- SYNC LED is amber: Indicates a Holdover or Acquiring state.
- SYNC LED is off: Indicates synchronization in disable or free-running state.

The following table desribes the implication of LED light status of GPS, BITS port, and SYNC LEDs.

Table 3: LED Light States

LED Type	LED State	Description
GPS	Green	The GPS interface is provisioned and frequency, time of day, and phase input is operating accurately.
	Off	The GPS interface is not provisioned or the GPS input is not operating accurately.
BITS port	Green	The BITS interface is provisioned and frequency is operating accurately.
	Off	The BITS interface is not provisioned or the BITS input is not operating accurately.
SYNC	Green	The frequency, time, and phase are synchronized to an external interface. The external interface can be: • BITS • GPS • Recovered RX clock
	Amber	The sytem is running in holdover or free-run mode and based on user configuration it is not synchronized to an external interface, as expected.
	Off	The centralized frequency or time and phase distribution is not enabled. Therefore, all clocking is based on the local oscillator on the RSP.

Building Integrated Timing Supply

Router supports receiving (Rx) and transmitting (Tx) of frequency via BITS interface. To receive and transmit BITS signals, configuration is done under the clock-interface sync 0 on the route processor (RP).

Note Both RP0 and RP1 should have identical configurations and should be connected to same external reference for sync 0 and sync 2 to meet phase transient response compliance standards during RP failover.

Prerequisite for BITS

Frequency synchronization must be configured with the required quality level option at the global level.

```
Router# show running-config frequency synchronization
Wed Aug 21 12:37:32.524 UTC
frequency synchronization
 quality itu-t option 1
!
```

Note BITS-In and BITS-Out on the peer nodes must be configured with the same mode and format.

Configuring BITS-IN

```
Router# configure
Wed Aug 21 12:29:59.162 UTC
Router(config)# clock-interface sync 0 location 0/RP0/CPU0
Router(config-clock-if)# port-parameters
Router(config-clk-parms)# bits-input e1 crc-4 sa4 ami
Router(config-clk-parms)# exit
Router(config-clock-if)# frequency synchronization
Router(config-clk-freqsync)# selection input
Router(config-clk-freqsync)# wait-to-restore 0
Router(config-clk-freqsync)# priority 1
Router(config-clk-freqsync)# commit
Wed Aug 21 12:30:53.296 UTC

Router# show running-config clock-interface sync 0 location 0/RP0/CPU0
Wed Aug 21 12:31:43.350 UTC
clock-interface sync 0 location 0/RP0/CPU0
 port-parameters
  bits-input e1 crc-4 sa4 ami
 !
 frequency synchronization
  selection input
  priority 1
  wait-to-restore 0
 !
!
```

Configuring BITS-OUT

```
Router# configure
Wed Aug 21 12:53:24.189 UTC
Router(config)# clock-interface sync 0 location 0/RP0/CPU0
Router(config-clock-if)# port-parameters
Router(config-clk-parms)# bits-output e1 crc-4 sa4 ami
Router(config-clk-parms)# commit
```

```
Wed Aug 21 12:53:39.411 UTC

Router# show running-config clock-interface sync 0 location 0/RP0/CPU0
Wed Aug 21 12:54:02.853 UTC
clock-interface sync 0 location 0/RP0/CPU0
 port-parameters
  bits-output e1 crc-4 sa4 ami
 !
!
```

Note Based on the quality level chosen in global configuration, E1/T1 modes can be changed as required. But in all the cases, both TX and RX side modes and submodes must be the same.

For non-CRC-4/D4 modes, SSM is not present in BITS and manual receive quality level must be configured.

Verifying BITS-IN Configuration

```
Router# show controllers timing controller clock
Wed Aug 21 12:38:20.394 UTC

SYNCC Clock-Setting: 1 -1 -1 -1

          Port 0          Port 1          Port 2          Port 3
Config     : Yes            No              No              No
Mode       : E1             -               -               -
Submode1   : CRC-4          -               -               -
Submode2   : AMI            -               -               -
Submode3   : 0              0               0               0
Shutdown   : 0              0               0               0
Direction  : RX             RX/TX           RX/TX           RX/TX
Baud-Rate  : -              -               -               -
QL Option  : O1             O1              -               -
RX_ssm(raw): 99             -               -               -
TX_ssm     : -              -               -               -
If_state   : UP           DOWN            DOWN            DOWN
```

Verifying BITS-OUT Configuration

```
Router# show controllers timing controller clock
Wed Aug 21 12:49:32.923 UTC
SYNCC Clock-Setting: 1 -1 -1 -1

          Port 0          Port 1          Port 2          Port 3
Config     : Yes            No              No              No
Mode       : E1             -               -               -
Submode1   : CRC-4          -               -               -
Submode2   : AMI            -               -               -
Submode3   : 0              0               0               0
Shutdown   : 0              0               0               0
Direction  : TX             RX/TX           RX/TX           RX/TX
Baud-Rate  : -              -               -               -
QL Option  : O1             O1              -               -
RX_ssm(raw): -              -               -               -
TX_ssm     : 22             -               -               -
If_state   : UP             DOWN            DOWN            DOWN
```

Verify Quality Level Received and Clock Interfaces

```
Router# show frequency synchronization clock-interfaces brief
Tue Feb 23 23:42:22.654 UTC
```

```
Flags: > - Up               D - Down                         S - Assigned for selection
d - SSM Disabled            s - Output squelched             L - Looped back
Node 0/RP0/CPU0:
==============
Fl      Clock Interface        QLrcv    QLuse    Pri   QLsnd    Output driven by
=====   ====================   ======   ======   ===   ======   ========================
D       Sync0                  n/a      n/a      n/a   n/a      n/a
D       Sync1                  n/a      n/a      n/a   n/a      n/a
>S      Sync2                  None     PRC      100   n/a      n/a
>S      Internal0              n/a      SEC      255   n/a      n/a
Node 0/RP1/CPU0:
==============
Fl      Clock Interface        QLrcv    QLuse    Pri   QLsnd     Output driven by
=====   ====================   ======   ======   ===   ======    ========================
D       Sync0                  n/a      n/a      n/a   n/a       n/a
D       Sync1                  n/a      n/a      n/a   n/a       n/a
D       Sync2                  n/a      n/a      n/a   n/a       n/a
>S      Internal0              n/a      SEC      255   n/a       n/a
```

Verifying the Frequency Synchronization Configuration

After performing the frequency synchronization configuration tasks, use this task to check for configuration errors and verify the configuration.

SUMMARY STEPS

1. **show frequency synchronization configuration-errors**
2. **show frequency synchronization interfaces brief**
3. **show frequency synchronization interfaces** *node-id*
4. **show processes fsyncmgr location** *node-id*

DETAILED STEPS

Step 1 show frequency synchronization configuration-errors

Example:

```
Router# show frequency synchronization configuration-errors

Node 0/2/CPU0:
==============
  interface HundredGigE 0/2/0/0 frequency synchronization
    * Frequency synchronization is enabled on this interface, but isn't enabled globally.

  interface HundredGigE 0/2/0/0 frequency synchronization quality transmit exact itu-t option 2
generation 1 PRS
    * The QL that is configured is from a different QL option set than is configured globally.
```

Displays any errors that are caused by inconsistencies between shared-plane (global) and local-plane (interface) configurations. There are two possible errors that can be displayed:

- Frequency Synchronization is configured on an interface (line interface or clock-interface), but is not configured globally. Refer to Enabling Frequency Synchronization on the Router, on page 3

- The QL option configured on some interface does not match the global QL option. Under an interface (line interface or clock interface), the QL option is specified using the **quality transmit** and **quality receive** commands. The value specified must match the value configured in the global **quality itu-t option** command, or match the default (option 1) if the global **quality itu-t option** command is not configured.

Once all the errors have been resolved, meaning there is no output from the command, continue to the next step.

Step 2 **show frequency synchronization interfaces brief**

Example:

```
Router# show frequency synchronization interfaces brief

Flags:  > - Up                D - Down              S - Assigned for selection
        d - SSM Disabled      x - Peer timed out    i - Init state

Fl  Interface                QLrcv QLuse Pri QLsnt Source
=== ======================== ===== ===== === ===== ========================
>Sx HundredGigE 0/2/0/0   Fail  Fail  100 DNU   None
Dd  HundredGigE 0/2/0/1   n/a   Fail  100 n/a   None

Router# show frequency synchronization clock-interfaces brief

Flags:  > - Up                D - Down              S - Assigned for selection
        d - SSM Disabled      s - Output squelched  L - Looped back

Node 0/0/CPU0:
==============
  Fl    Clock Interface     QLrcv  QLuse  Pri QLsnd  Source
  ===== =================== ====== ====== === ====== ========================
  >S    Sync0               PRC    Fail   100 SSU-B  Internal0 [0/0/CPU0]
  >S    Internal0           n/a    SSU-B  255 n/a    None

Node 0/1/CPU0:
==============
  Fl    Clock Interface     QLrcv  QLuse  Pri QLsnd  Source
  ===== =================== ====== ====== === ====== ========================
  D     Sync0               None   Fail   100 SSU-B  Internal0 [0/1/CPU0]
  >S    Internal0           n/a    SSU-B  255 n/a    None
```

Verifies the configuration. Note the following points:

- All line interface that have frequency synchronization configured are displayed.
- All clock interfaces and internal oscillators are displayed.
- Sources that have been nominated as inputs (in other words, have **selection input** configured) have ‘S’ in the Flags column; sources that have not been nominated as inputs do not have ‘S’ displayed.

  Note Internal oscillators are always eligible as inputs.

- ‘>’ or ‘D’ is displayed in the flags field as appropriate.

If any of these items are not true, continue to the next step.

Step 3 **show frequency synchronization interfaces** *node-id*

Example:

```
Router# show frequency synchronization interfaces HundredGigE 0/2/0/2
```

```
Interface HundredGigE 0/2/0/2 (shutdown)
  Assigned as input for selection
  SSM Enabled
  Input:
    Down
    Last received QL: Failed
    Effective QL:     Failed, Priority: 100
  Output:
    Selected source:    Sync0 [0/0/CPU0]
    Selected source QL: Opt-I/PRC
    Effective QL:       Opt-I/PRC
  Next selection points: LC_INGRESS

Router# show frequency synchronization clock-interfaces location 0/1/CPU0

Node 0/1/CPU0:
==============
  Clock interface Sync0 (Down: mode not configured)
    SSM supported and enabled
    Input:
      Down
      Last received QL: Opt-I/PRC
      Effective QL:     Failed, Priority: 100
    Output:
      Selected source:    Internal0 [0/1/CPU0]
      Selected source QL: Opt-I/SSU-B
      Effective QL:       Opt-I/SSU-B
  Next selection points: RP_SYSTEM

  Clock interface Internal0 (Up)
    Assigned as input for selection
    Input:
      Default QL:   Opt-I/SSU-B
      Effective QL: Opt-I/SSU-B, Priority: 255
  Next selection points: RP_SYSTEM RP_CLOCK_INTF
```

Investigates issues within individual interfaces. If the clock interface is down, a reason is displayed. This may be because there is missing or conflicting platform configuration on the clock interface.

Step 4 **show processes fsyncmgr location** *node-id*

Example:

```
Router# show processes fsyncmgr location 0/0/CPU0

                  Job Id: 134
                     PID: 30202
        Executable path: /pkg/bin/fsyncmgr
             Instance #: 1
             Version ID: 00.00.0000
                Respawn: ON
          Respawn count: 1
  Max. spawns per minute: 12
           Last started: Mon Mar  9 16:30:43 2009
          Process state: Run
          Package state: Normal
      Started on config: cfg/gl/freqsync/g/a/enable
                   core: MAINMEM
               Max. core: 0
               Placement: None
            startup_path: /pkg/startup/fsyncmgr.startup
```

```
                Ready: 0.133s
      Process cpu time: 1730768.741 user, -133848.-361 kernel, 1596920.380 total
-------------------------------------------------------------------------------
```

Verifies that the fsyncmgr process is running on the appropriate nodes.

Support for ITU-T G.8264 Standard

Table 4: Feature History Table

Feature name	Release Information	Feature Description
Support for ITU-T G.8264 Standard	Release 7.3.1	The Ethernet Synchronization Message Channel (ESMC) protocol is specified in the ITU-T G.8264 performance compliance standard. It provides recommendations on synchronizing clock frequency across a network over an Ethernet port, along with the ability to select quality levels. The G.8264 standard provides a new extended Quality Level (QL) of Type Length Value (TLV). As Ethernet equipment gradually replace SONET and SDH equipment in service provider networks, frequency synchronization provides high-quality clock synchronization over Ethernet ports.

The Ethernet Synchronization Message Channel (ESMC) protocol specified in the ITU-T G.8264 enables the synchronization of clock frequency across a network over Ethernet ports with the ability to select enhanced quality levels. Enhanced quality levels lead to improved bandwidth, frequency accuracy, and holdover along with reduced noise generation in a network.

As part of the ESMC protocol, the quality level (QL) of timing signals is distributed through Synchronization Status Messages (SSMs). The updated G.8264 standard provides a new and enhanced Quality Level (QL) of Type Length Value (TLV) that allows more precise quality to provide accurate clocks.

The new and enhanced QL of TLV that is part of the updated G.8264 standard is known as enhanced SyncE (eSyncE). The enhanced QL of TLV enables support for more QL values. You can configure a router to send or receive the enhanced TLV. The enhanced QL of TLV results in more precise synchronization of clocks across a network. To enable this feature, the local clock ID is configured. The clock ID is used, when appropriate, in the extended QL TLVs

Note Default clock ID is based on the MAC address of the chassis.

Restrictions

There may be devices in a network that do not support eSyncE and also do not support enhanced ESMC. If a router does not support eSyncE, it ignores any enhanced TLVs it receives and does not support enhanced quality to provide accurate clocks. Such routers at ingress nodes drop the QL TLV received from the previous node supporting eSyncE. If the next node supports enhanced ESMC, then the extended QL TLV is applied afresh to that node.

Configuration

1. Configure frequency synchronization on the router.
2. Configure the MAC address of the device clock that can transmit the enhanced QL TLV in the network.
3. Configure frequency synchronization on an interface.
4. Configure the quality level options to be transmitted by the device clock.

Configuration Example

```
/* Configure frequency synchronization on the router. */
Router# configure
Router(config)# frequency synchronization

/* Configure the MAC address of the clock that can transmit the enhanced QL TLV in the
network. */
Router(config-freqsync)# clock-id mac-address 0000.0001.0003
Router(config-freqsync)# commit
Router(config-freqsync)# exit

/* Configure frequency synchronization on an interface. */
Router(config)# interface HundredGigE 0/1/0/0
Router(config-if)# frequency synchronization

/* Configure the quality level options to be transmitted by the device clock. */
Router(config-if-freqsync)# quality transmit exact itu-t option 1 ePRTC
```

Running Configuration

```
Router# show running-config
frequency synchronization
 clock-identity mac-address 0000.0001.0003
!
interface preconfigure HundredGigE 0/1/0/0
 frequency synchronization
  quality transmit exact itu-t option 1 ePRTC
 !
!
```

Verification

To verify if eSyncE is configured, use the **show frequency synchronization interfaces** command.

```
Router# show frequency synchronization interfaces
Interface HundredGigE 0/11/0/1 (up)
  Assigned as input for selection
  Wait-to-restore time 0 minutes
  SSM Enabled
    Peer Up for 00:00:54, last SSM received 0.741s ago
    Peer has come up 1 times and timed out 0 times
    ESMC SSMs        Total  Information     Event    DNU/DUS
      Sent:             55           53         2         45
      Received:         55           55         0          0
  Input:
    Up
    Last received QL: Opt-I/ePRTC
    Effective QL: Opt-I/ePRTC, Priority: 30, Time-of-day Priority 100
    Originator clock ID: aaaabbfffebbcccc
    SyncE steps: 1, eSyncE steps: 1
    All steps run eSyncE; Chain of extended ESMC data is complete
    Supports frequency
  Output:
    Selected source: HundredGigE 0/11/0/1
    Selected source QL: Opt-I/ePRTC
    Effective QL: DNU
    Originator clock ID: aaaabbfffebbcccc
    SyncE steps: 2, eSyncE steps: 2
    All steps run eSyncE; Chain of extended ESMC data is complete
  Next selection points: ETH_RXMUX
```