Paging eDRX H-SFN Changed to 10 Bits Counter

Feature Summary and Revision History

Summary Data

Applicable Product(s) or Functional Area	MME
Applicable Platform(s)	• ASR 5500 • VPC-DI • VPC-SI
Feature Default	This feature is enabled/disabled, when the eDRX feature is enabled/disabled.
Related Changes in This Release	Not applicable
Related Documentation	*MME Administration Guide*

Revision History

Revision Details	Release
Paging eDRX H-SFN changed to 10 bits counter introduced in release 21.13.	21.13.11
Paging eDRX H-SFN changed to 10 bits counter introduced in release 21.11.	21.11.3
Paging eDRX H-SFN changed to 10 bits counter introduced in release 21.12.	21.12.5
First introduced.	21.0

Feature Changes

Previous Behavior: Paging eDRX H-SFN is 32 bits counter.

New Behavior: Paging eDRX H-SFN changed to 10 bits counter to allow values between 0 to 1023 as per 3GPP TS 36.331 V13.13.0.

Customer Impact: Customer can see the change in the paging timings.